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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,006	02/16/2001	Aaron Schoenfeld	303.259US3	5063

7590 03/26/2004

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/785,006	SCHOENFELD, AARON	
	Examiner	Art Unit	
	Evan Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-25,35-39 and 41-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-25,35-39 and 41-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. The restriction requirement mailed April 1, 2003 is withdrawn.

Species II and I are rejoined with claims 11-25, 35-39 and 41-43 pending.

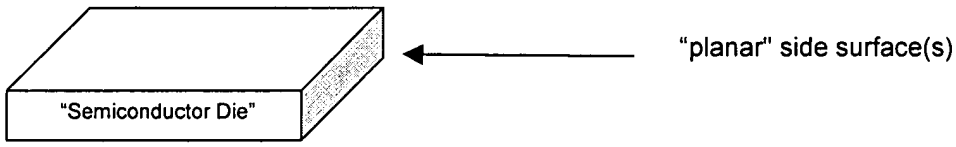
As a reminder, Species I and Species II are repeated:

Species I = "Semiconductor die" having "stepped edge" (i.e. "bi-level edge")

[e.g. claims 18-25, 35-39 and 41-43 are "readable on" Species I].

Species II = "Semiconductor die" having "planar perimeter side surfaces" that extend between major faces of the semiconductor die.

[e.g. claims 11-17 are "readable on" Species II].



Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11-16, 18-25, 35-38 and 41-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant's attempt to definitively claim *surface quality* by writing, "ground or polished" in the claims and suggesting "CMP" in the specification for "ground or polished," renders the claims ambiguous:

The term "ground or polished surface" (i.e. a subjective description of *surface quality*), is not a definitive term, but is rather a relative term of degree, depending on the *quantitative* meaning of things like the roughness, smoothness, type of imperfections, damage, nature of scratches, and the generally process-residual artifacts that constitute a "ground or polished surface."

Applicant certainly doesn't disclose adequate *specifics* of a grinding or polishing *process* that would clearly define a scope of a "ground or polished" *surface quality* [MPEP 2113]. What cutting tool? What grinding tool? What type and size grit? What pressure? What speed? What coolant? Applicant generally directs one to: "cut" and then "grind or polish" such as by "CMP."

Applicant attempts to define "ground or polished" *surface quality* in relative terms of "increasing the smoothness and flatness," [e.g. p. 7, line 2] and "reducing or eliminating irregularities" [e.g. p. 7, line 5], which renders the claims ambiguous with respect to actual *surface quality* of the surface(s) being claimed.

Based on the relative terms of "reducing" and "increasing", applicant urges that the "ground or polished" claim language must be taken from the specification as being a clear and concise way of describing a specific surface quality of the finally claimed surfaces shown in gray depicting Species I and Species II above.

Yet, in the specification, "ground or polished" is disclosed as "ground or polished smoother and flatter with less irregularities than something else," such that applicant's claimed "ground or polished" surface is an ambiguous surface, ground or polished by any process *or inadvertent consequence,* or just simply appearing to have been ground or polished in some way.

Since applicant fails to develop or refer to a measurable standard of *surface quality* for "ground or polished," for purposes of examination, any surface formed by a "grinding" operation is reasonably considered as being a "ground or polished surface."

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 11-12, 14-16 and 18, 20-25, 35-36, 38, 41 and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Boruta (U.S. 5,786,266) in view of secondary references comprising Efrat et al. (1995), Weisshaus et al. (2001) and Boucher et al. (U.S. 5,718,615), for showing a *universal fact* [See MPEP 2124].

The cited secondary references to Boruta teach the *universal fact* that necessarily holds true in Boruta: Boruta's disclosed methodology of making cuts by a "dicing" saw is inherently a "grinding" resulting in a "ground surface" [see introductions to each of the three secondary references].

Boruta discloses a multi cut wafer saw process that forms a semiconductor die 30 having bi-level side *surface orientations*, for anticipation of the claim limitations drawn to the orientation of bi-level side surface(s) that define Species II [Fig. 2D].

Boruta discloses a prior art single cut wafer saw process that forms a semiconductor die10 having planar side *surface orientations*, for anticipation of the claim limitations drawn to side surface(s) that define Species I [Fig. 1B].

Boruta calls the "multi cut wafer saw process" a "dicing" process, which, by *universal fact*, is a "grinding process" resulting in a "ground surface" [Weisshauss teaches "ground surface," for example].

Since the *surface orientations* disclosed by Boruta clearly anticipate the *surface orientations* for claimed Species I and Species II die, and the act of "dicing" is an act of "grinding" resulting in a "ground surface," the side surfaces of the die in Fig. 1B and 2D of Boruta are necessarily and inherently "ground *or* polished."

Furthermore, the semiconductor dies disclosed by Boruta each *inherently* "have circuitry on the upper surface" because there are semiconductor devices on the upper surface with test patterns in the scribe lines between the pre-cut die so in every situation there must be "circuitry" found on the top since "circuitry" necessarily forms the electrical pathways of the "semiconductor devices" [col. 1, line 15].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11-12, 14-18, 20-25, 35-36, 38-39, 41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boruta (w/ secondary references), as applied to claims 11-25, 35-38 and 41-43 above, and further in view of Bean et al., optionally taken with Borneman et al. (U.S. 3,152,939).

Boruta is silent about a "polished side surface" of the die depicted in Figs. 1B and 2D. These die disclosed in Boruta *inherently* have ground side surfaces, as established *supra*, but do not necessarily have the equivalent of (a) "polished side surface(s)."

Bean et al.'s invention is highly relevant because Bean et al. is all about cutting and separating semiconductor die from a wafer, wherein Bean discloses to the reader that edge roughness of any prior art cut (diced) die can be "smoothed somewhat by polishing after dicing" [col. 2, lines 18-19].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to polish the side surfaces of the die of Fig. 1B and/or 2D of Boruta. One of ordinary skill would be motivated by the teaching of Bean et al. that "polishing the side surfaces" is a way that "edge roughness may be smoothed" [col. 2, line 17].

While Bean et al. directs one to polishing sides of a semiconductor die, the polishing disclosed in Bean et al. might wrongly be interpreted as being solely for the invention of Bean et al., so the examiner cites a seminal dicing patent to Borneman et al., for additional motivation to polish away edge roughness, which teaches:

> Cutting the wafers into dice introduces saw damage along the edges of the dice which must be removed...[col. 1, lines 27-29, emphasis added].

Therefore, Borneman et al. discloses an old teaching that "dicing saw damage must be removed" when a dicing saw cut (inherently a grind) is used.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to polish the sides of the die in Boruta's Fig. 1B and 2D, motivated by the teachings of Borneman et al., that sawing damage must be removed, and Bean et al., who teaches that polishing reduces the dicing saw damage edge roughness of a dicing saw's inherently grinding cut.

6. Claims 13, 19, 37 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boruta with secondary references as applied to claims 11, 18, 35 and 41 above, and further in view of Natsume (U.S. 5,477,062).

Boruta is silent about semiconductor die being "rectangular" because Boruta is silent about scribe lines being "perpendicular" as is practiced in the vast majority of prior art, and Boruta doesn't show a top view of the semiconductor die.

Rectangular die are the most common shape, so Boruta isn't expected to talk about that which is so incredibly well known to the rudimentary of skill:

Natsume shows the notoriously well-known shape of a "rectangle" for a "semiconductor die" in Fig. 1A. This is the shape that Natsume chooses like so many do in the art. It would have been obvious to one of ordinary skill in the art to use the multi cut dicing method of Boruta, motivated to solve the same problem as Natsume, but in an alternative manner such that the necessary test element patterns in the scribe lines of Natsume can take on any form, rather than be limited by the specifics of the test patterns taught by Natsume.

Response to Arguments

7. Applicant's arguments with respect to claims 18-25, 35-39 and 41-43 have been considered but are moot in view of the new grounds of rejection.

8. The examiner notes applicant's following statement with interest:

> **Applicant does NOT assert or admit that the claims cover *only* a surface formed by cutting and then treating** [paper received 1-12-04, page 10].

The examiner agrees that treating after cutting isn't the only way to have a "ground or polished surface"; for example, *dicing* by grinding with a diamond grit-impregnated dicing wheel, results in a "ground surface" even though applicant insists it is a relatively more damaged ground surface than applicant's grinding.

9. Applicant paradoxically insists that "ground or polished" is not a product-by-process limitation in terms of MPEP 2113:

Yet, applicant's argument contradicts claim 22, for example, where the surface is "ground or polished *to remove irregularities*." Applicant's argument that "ground or polished" is not a "product-by-process" limitation does not make logical sense; since something *necessarily* "*was* ground" in order, "to remove" some irregularities.

A surface can logically be designated as "ground or polished" only when a "grinding or polishing" operation created the "ground or polished" surface quality. Applicant, as the only example, refers to a well-known process called CMP (chemical-mechanical-polishing) for the suggested process of grinding or polishing, to get a "ground or polished surface."

As is known to anyone who practices CMP, CMP leaves striations and imperfections, depending on grit size, pad pressure, and other parameters, just like the striations and imperfections of "surface morphology" seen from a grinding cut of a semiconductor die diced from a wafer [See Introduction to Kim et al. with views of "ground surfaces" at Fig. 3, 4 and 9].

10. Applicant's arguments continue to obscure the plain meaning of a "ground surface": Undoubtedly, a "ground surface" can reasonably be a "ground surface evidenced by scratches" or a "ground surface that has fracturing at an edge" or a "ground surface with cracks leading away from the edge", among a plethora of other grinding-artifact descriptions. Likewise, a "polished surface" can be an imperfect surface (how polished is it?).

Without using the words "ground or polished", can applicant *quantify* the claimed *surface quality* compared to *inherent* surface qualities of the prior art?

11. The ordinary of skill *know* the meaning of a "polished" semiconductor wafer only by parameters that *quantify* a polished *surface quality,* such as TTV, number of scratches, parallelism and the like [e.g. See SEMI Standard M8-93].

How does applicant quantify the surface quality being claimed besides ambiguously writing, "ground or polished"? Applicant's grinding-after-cutting operation *necessarily* causes damage because grinding a semiconductor crystal is a machining operation of a brittle material [See Introduction to Marshall et al., starting at p. 461]. How does the damage from applicant's grinding compare to the damage from grinding in Boruta, in quantitative terms?

12. The examiner acknowledges applicant's statement:

Applicant reserves the right to swear behind any references... [p. 8, bottom].

The examiner does not understand the need to "reserve the right" because applicant is already entitled to swear behind references under Rule 131.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

John Wiley & Sons Encyclopedia, Chapter 5 entitled "Chips" is cited for those unfamiliar with "cutting" a "semiconductor die" from a "wafer" by the grinding action of a diamond-coated blade. Fig. 5.20 shows that ground surface quality can vary greatly [see Figs. 5.17, 5.18, 5.19 and 5.20 at p. 94-95].

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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March 11, 2004